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ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E. /B.Tech / B. Arch (Full Time) - END SEMESTER EXAMINATIONS, May 2025

Name of the Branch: Electronics and Communication Engineering
Semester: VI
Subjectcode&SubjectTitle: EC5015- Data Converters
(Regulation2019)

Time:3hrs Max.Marks: 100

CO1	To design MOS circuits applied for various data conversion stages namely, sample and hold, comparators, switched capacitor amplifiers
CO2	To, study the various CMOS design considerations of ADC architectures used in practice• including SAR, Pipeline, Flash ADCs
CO3	To study the general design principles design sigma delta converters•

BL – Bloom's Taxonomy Levels
(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

PART- A(10x2=20Marks)
(Answer all Questions)

Q.No	Questions	Marks	CO	BL
1	The spectrum of a continuous time signal and its spectrum after sampling are shown in Fig. 1. What are the possible frequencies corresponding to the smaller arrows in the spectrum of the continuous time signal.	2	1	L2
2	Applying a ramp signal (periodic sawtooth) at the input of a quantizer produces the quantization noise e_q as shown in Fig.2. Show that the average power of the quantization noise is given by $e_q^2 = \Delta^2/12$	2	1	L4
3	What is the functionality of the circuit shown in Fig.3. If some external components are to be connected to realize the functionality, indicate the same.	2	1	L2
4	Explain how sampling time errors are introduced due to input variation of input voltage in a simple track and hold circuit.	2	1	L1
5	Why is does one need the capacitor structure to be of the type shown in Fig.4. Draw the possible field lines of this capacitor.	2	1	L1
6	Sketch the input-output transfer characteristics of any ideal comparator. Also show how this characteristic will get modified if the comparator suffers from offset.	2	1	L1
7	Explain what is meant by kick back noise in comparators.	2	3	L2
8	Derive the expression for the transfer function V(z)/U(z) for the circuit shown in Fig.5	2	3	L4
9	By simply oversampling without feedback followed by digital filtering, show that one can improve the bit resolution of any quantizer by ½ bit for every doubling of the sampling frequency (half a bit per octave rule).	2	2	L4
10	Explain why one needs to use Windowing of the samples while testing the performance of ADCs	2	2	L1

PART- B(5x 13=65Marks)
(Restrict to a maximum of 2 subdivisions)

Q.No	Questions	Marks	CO	BL
11 (a) (i)	Fig6a and Fig.6b show the spectra of a continuous time signal and its	8	1	L5

	sampled time version respectively. Give the full range of frequencies of the interfering tone for which aliasing will not occur. Suggest two different ways by which in this aliasing of the interfering tone can be reduced or eliminated. Next, suggest ways by which the interfering tone after aliasing will be guaranteed to be kept 40dB below the desired signal.			
11 (a)(ii)	Explain how you would use a capacitor array to realize a 3 bit D to A converter.	**5**		
	OR			
11(b) (i)	The expression given below arises in the context of reconstruction of a continuous time analog signal from discrete time samples. Assume any bandlimited spectrum of your choice for X(f) and sketch the spectrum of Xp(f). What are the possible extreme values for Tp and how does the spectrum of Xp(f) will get altered for these two extremes. How does one recover the original spectrum X(f) from Xp(f). $X_p(f)=\frac{T_p}{T_s}\frac{\sin(\pi f T_p)}{\pi f T_p}\cdot e^{-j\pi f T_p}\sum_{n=-\infty}^{\infty} X\left(f-\frac{n}{T_s}\right)$	**7**	1	L5
11(ii))	Draw the circuit diagram any 4 bit binary weighted current steering DAC and determine the worst case glitch amplitude .	**6**		
12 (a) (i)	Consider the issue of clock feedthrough as depicted in Fig.7. Show that the expression for gain and offset errors due to clock feedthrough are given respectively by $\varepsilon = -C_{OL}/(C+C_{OL})$ and $Vos = -\{C_{OL}/(C+C_{OL})\} \times (V_{th}-\Phi_L)$	**6**	1	L4
(ii)	For the track and hold circuit shown in Fig.8, ignoring clock feedthrough and assuming fast gating, show that the expressions for gain and offset errors are given respectively by $\varepsilon=\frac{1}{2}\frac{WLC_{ox}}{C}$ $V_{os}=-\frac{C_{ol}}{C_{ol}+C}(\phi_H-\phi_L)-\frac{1}{2}\frac{WLC_{ox}}{C}(\phi_H-V_t)$	**7**		
	OR			
12 (b) (i)	For Fig. 9, sketch the waveforms for the clocks Φ1, Φ2, Φ3, and Φ4. Which transistors contribute to charge injection error. Assume fast gating and show that the expression for the output voltage is as given below and give the expression for ΔQ $V_{out}=\frac{C}{C_f}V_{in}+\frac{\Delta Q}{C_f}$	**7**	1	L4
12(b) (ii)	In Fig.10 what is the function of the various transistors. Why are the dimensions some transistors different from others. What is the possible thermal noise voltage limit set by the tracking capacitor in this circuit.	**6**		
13 (a)	In the circuit in Fig.11, indicate which terminals should be marked as Vop and Von respectively. When latch is set as zero indicate the voltages at the drains of transistors M2b and M2a. List all transistors that are in the cutoff state during latch equal to zero. In this circuit, suggest how one can reduce the regeneration time constant. Assuming V_{IN} is greater than V_{IP}, draw a rough sketch to indicate the evolution of the voltages at the drains of M2a and Mb.	**13**	1	L3
	OR			

13 (b) (i)	For a B bit Flash ADC with the comparators using a preamp of gain Av, derive an expression for the probability of entering into a metastable state. Assume full scale input is VDD	**6**	1	L3
13(b) (ii)	In Fig. 12, assume In+ is greater than In-. Determine the voltages at nodes A, B and Out+ and Out- during Clk = 0 and during Clk =VDD.	**7**		
14 (a)	Draw the circuit diagram of a single ended 5 bit SAR ADC and show the capacitor array sizes and switching scheme clearly. Provide the necessary expressions to show that the scheme carries out the binary search algorithm to arrive the final output digital word corresponding to the input analog signal. What are the considerations that go into choosing the size of the minimum value of the capacitor.	**13**	3	L3
	OR			
14 (b) (i)	Fig.13 shows the capacitor array for a 4bit differential SAR. Assume Vin+ =0.6V, Vin- =0.4V and VDD=1.0V. Explain how the search procedure is carried out and what is the final 4bit word of the digital output. In the present scheme, for every input analog sample, explain how many clock cycles are needed to arrive at final output digital word.	**10**	3	L3
14(b) (ii)	Explain how sampling error due to jitter can be reduced in a track and hold circuit.	**3**		
15 (a)	In Fig.14, determine the expressions for the Noise Transfer Functions of N1(z), N2(z) and E(z). Hence show that the equivalent input mean square noise due to N1 and N2 alone is given by $\overline{v_{in,tot}^2} = \overline{v_{in,tot1}^2} \cdot \frac{1}{OSR} + \overline{v_{in,tot2}^2} \cdot \frac{\pi^2}{3} \frac{1}{OSR^3}$	**13**	2	L3
	OR			
15 (b)	Determine the expression for Y(z) in Fig.16 and Fig.17	**6+7**	2	L3

PART- C(1x 15=15Marks)

(Q.No.16 is compulsory)

Q.No	Questions	Marks	CO	BL
16. (i)	State the number of comparators and capacitors and switches required to build a single 16 bit SAR ADC.	**5**	1+3	L5+L6
16 (ii)	For an ADC, explain the terms DNL and INL along their expressions and also give the relation between them	**5**		
16(iii)	Show that the expression for the SQNR of the sigma delta converter show in Fig.18 is given by SQNR = -3.4+30log(M) where M is the sampling ratio.	**5**		

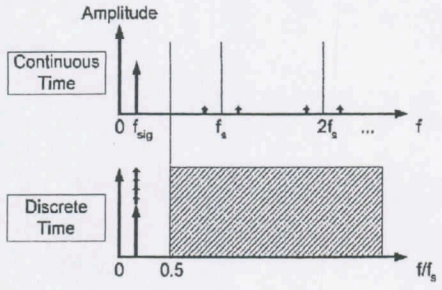

Fig.1

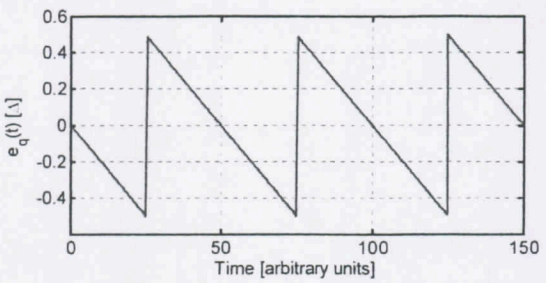

Fig.2

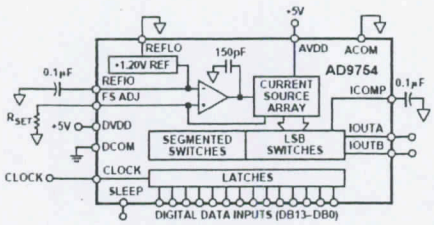

Fig.3

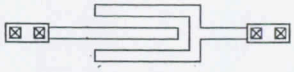

Fig.4

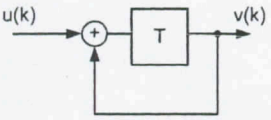

Fig.5

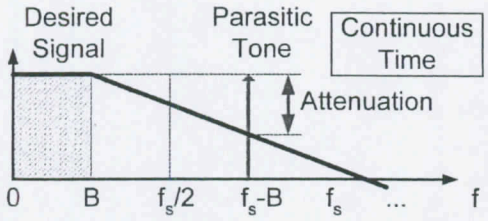

Fig.6a

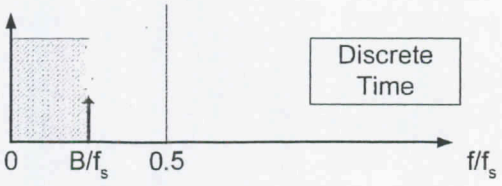

Fig.6b

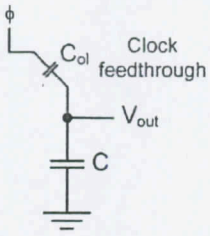

Fig.7

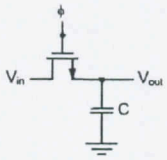

Fig.8

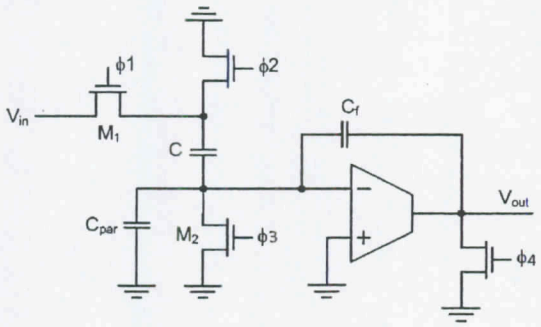

Fig9

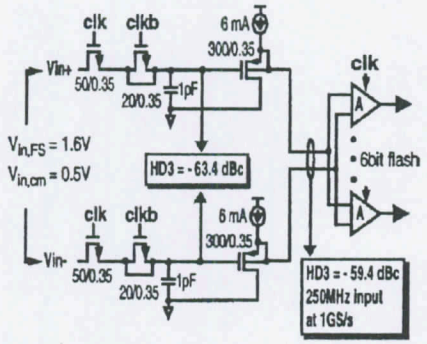

Fig.10

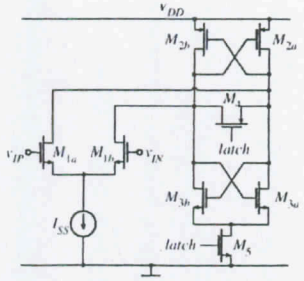

Fig.11

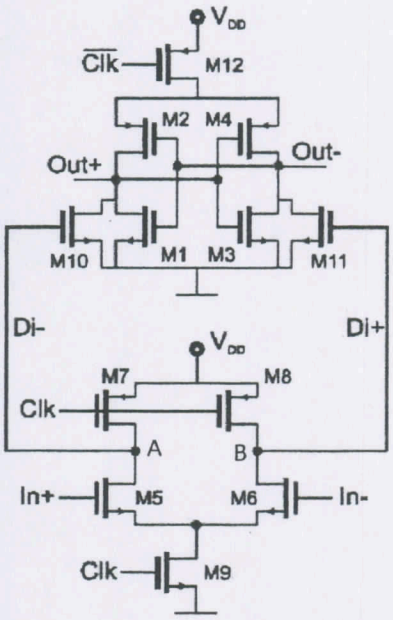

Fig.12

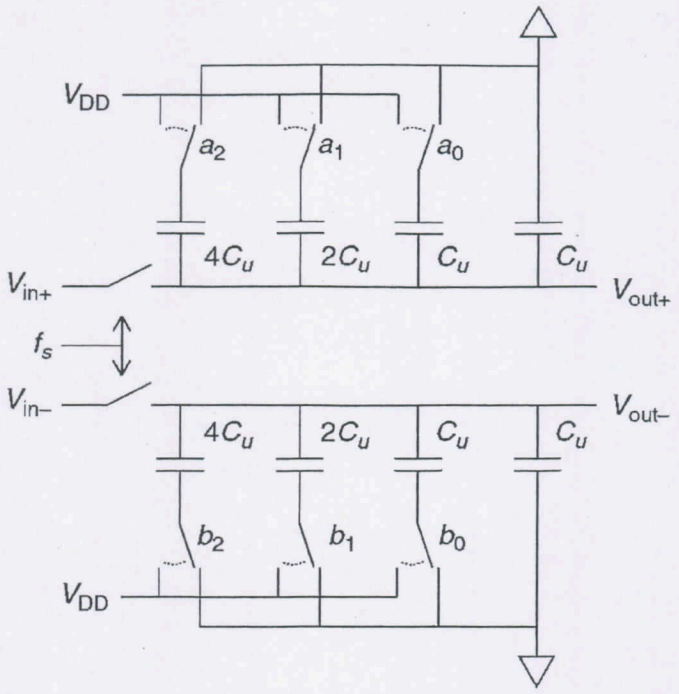

Fig.13

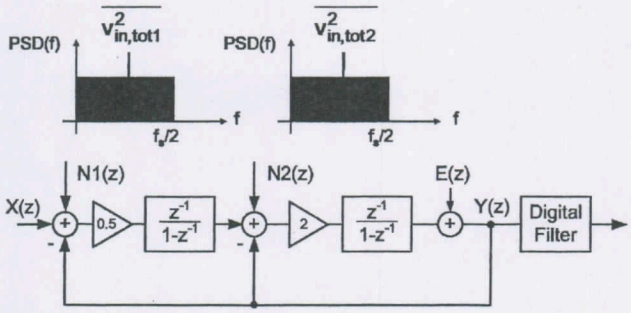

Fig.14

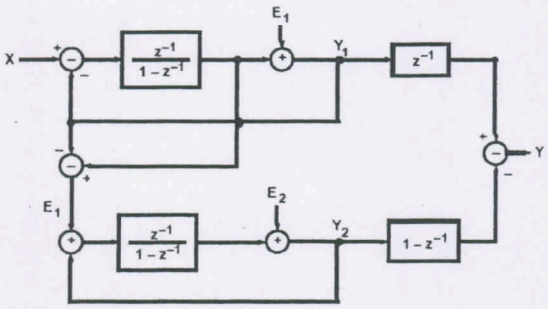

Fig.15

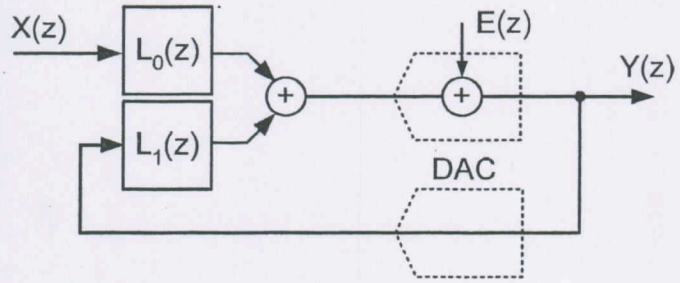

Fig.17

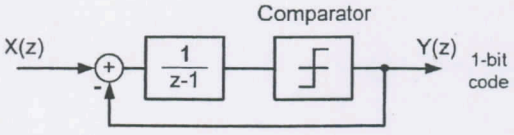

Fig.18